GPR (General Purpose Registers)

63		31		15	7	0
RAX	ACCUMULATOR	EAX	AX	AH	AL	
RCX	COUNT	ECX	CX	CH	CL	
RDX	DATA	EDX	DX	DH	DL	
RBX	BASE ADDRESS	EBX	BX	BH	BL	
RSP	STACK POINTER	ESP	SP	SPL		
RBP	BASE POINTER	EBP	BP	BPL		
RSI	SOURCE INDEX	ESI	SI	SIL		
RDI	DESTINATION INDEX	EDI	DI	DIL		
RIP	INSTRUCTION POINTER	EIP	IP			
RFLAGS		EFLAGS	FLAGS			
R8		R8D		R8W	R8B	
R9		R9D		R9W	R9B	
R10		R10D		R10W	R10B	
R11		R11D		R11W	R11B	
R12		R12D		R12W	R12B	
R13		R13D		R13W	R13B	
R14		R14D		R14W	R14B	
R15		R15D		R15W	R15B	

Segment Registers

15 0	
SS	STACK SEGMENT
DS	DATA SEGMENT
ES	EXTRA DATA SEGMENT
CS	CODE SEGMENT
FS	EXTRA DATA SEGMENT 2
GS	EXTRA DATA SEGMENT 3

MXCSR REGISTER

31	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	MM		FZ	RC		PM	UM	OM	ZM	DM	IM	DAZ	PE	UE	OE	ZE	DE	IE

FZ: FLush to Zero; RC: Rounding Control; PM: Precision Mask; UM: Underflow Mask; OM: Overflow Mask; ZM: Divide-by-Zero Mask; DM: Denormal Operation Mask; IM: Invalid Operation Mask; DAZ: Denormals Are Zeros; PE: Precision Flag; UE: Underflow Flag; OE: Overflow Flag; ZE: Divide-by-Zero Flag; DE: Denormal Flag; IE: Invalid Operation Flag

EFLAGS REGISTER

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED FOR INTEL										ID	VIP	VIF	AC	VM	RF	0	NT	IOPL		OF	DF	IF	TF	SF	ZF	0	AF	0	PF	1	CF

ID: Set/Unset CPUID; VIP: Virtual Interrupt Pending Flag; VIF: Virtual Interrupt Flag; AC: Alignment Check Flag; VM: Virtual 8086 Mode; RF: Resume Flag; NT: Nested Task; IOPL: I/O Privilege Level; OF: Overflow Flag; DF: Direction Flag; IF: Interrupt Enable Flag; TF: Trap Flag (cpu single step mode); SF: Sign Flag (result is negative); ZF: Zero Flag (result is zero); AF: Auxiliary Carry Flag; PF: Parity Flag (0=odd 1=even); CF: Carry Flag

FLAGS

HEX: #00**0F** **4F** **9D**h

LITTLE ENDIAN		BIG ENDIAN	
LOW MEMORY		LOW MEMORY	
LSB →	9D	MSB →	00
	4F		0F
	0F		4F
MSB	00	LSB	9D
HIGH MEMORY		HIGH MEMORY	

```
DB 5 DUP 0 ;DB 0,0,0,0,0
$          ;AKTUALNA ADRESA
```

	BITS	BYTES	DEFINE	RESERVE	RANGE	SIGN RANGE
BIT	1b				0-1	
NIBBLE	4b				0-15	
BYTES	8b	1B	DB	RB	0-255	-128 +127
WORD	16b	2B	DW,DU	RW	0-65535	-32768 +32767
DWORD single precision float	32b	4B	DD	RD	0-2↑32	-2↑31 +2↑31-1
FWORD,PWORD	48b	6B	DP,DF	RP,FR	0-2↑48	-2↑47 +2↑47-1
QWORD double precision float	64b	8B	DQ	RQ	0-2↑64	-2↑63 +2↑63-1
TWORD extended precision float	80b	10B	DT	RT	0-2↑80	-2↑79 +2↑79-1
DQWORD,OWORD4 floats	128b	16B			0-2↑128	-2↑127 +2↑127-1

15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
ST[7]	ST[6] ST[5] ST[4] ST[3] ST[2] ST[1] ST[0]

TAG

0 0	VALID NON-ZERO
0 1	ZERO
1 0	SPAC. VALUE (NaN, INFINITY)
1 1	EMPTY

Control registers

63	31	30	29	18	16	15	5	4	3	2	1	0	
	PG	CD	NW	AM	WP		NE	ET	TS	EM	MP	PE	MSW OLD 286
	PG	CD	NW	AM	WP		NE	ET	TS	EM	MP	PE	CR0 REZIM ADRESOVANIA
page fault virtual address													CR2 LIN. ADR. VYPADKU
52	51	PML4 base			12	11	PCD	PWT					CR3 FYZ. ADR. STRANOK
		11	OSXMMEX	OSFXSR	PCE	PGE	MCE	PAE	PSE	DE	TSD	PVI	VME CR4
											TPR		CR8
													CR15

Debug registers

31 LIN. ADR. VYKONANIA INT1 0	DR0
31 LIN. ADR. VYKONANIA INT1 0	DR1
31 LIN. ADR. VYKONANIA INT1 0	DR2
31 LIN. ADR. VYKONANIA INT1 0	DR3
	DR4
	DR5
31 STAVOVY REGISTER LADENIA INT1 0	DR6
31 PRIKAZOVY REGISTER LADENIA INT1 0	DR7
63 REGISTER ADRESY STROJOVEJ CHYBY 0	MCAR
63 REGISTER TYPU STROJOVEJ CHYBY 0	MCTR
63 TESTOVACI REGISTER 0	TR12

31 OFSET INSTRUKCIE CHYBY 0	FIP
31 **FOP** OPCODE 16 15 **FCS** SEGMENT 0	
31 OFSET OPERANDU INSTRUKCIE CHYBY 0	FOO
15 STAV FPU 0	SWR
31 **CWR** RIADENIE FPU 15 **FOS** SEG.ADR. 0	
15 **TAG** ZNACKY DAT 0	

Floating-Point Registers (10 BYTES TWORD)

	79	64	63	(8 BYTES QWORD 64b) MMX Registers	0
ST0				MM0	
ST1				MM1	
ST2				MM2	
ST3				MM3	
ST4				MM4	
ST5				MM5	
ST6				MM6	
ST7				MM7	

SSE (16 BYTES)

DQWORD | QWORD | DWORD | DWORD

127	XMM0	0
127	XMM1	0
127	XMM2	0
127	XMM3	0
127	XMM4	0
127	XMM5	0
127	XMM6	0
127	XMM7	0

SSE2 (16 BYTES) LONG MODE 64-BIT.

127	XMM8	0
127	XMM9	0
127	XMM10	0
127	XMM11	0
127	XMM12	0
127	XMM13	0
127	XMM14	0
127	XMM15	0

FLOAT | FLOAT | FLOAT | FLOAT
DOUBLE | DOUBLE

Control Word Register CWR FPU Control Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			IC	RC		PC		IEM		PM	UM	OM	ZM	DM	IM

IC: Infinity Control; RC: Rounding Control (zaokruhlovanie); PC: Precision Control (presnost vypoctu); IEM: Interupt Enable Mask; PM: Precision Mask; UM: Underflow Mask; OM: Overflow Mask; ZM: Zero divide Mask; DM: Denormal operand Mask; IM: Invalid Operation

Status Word Register SWR FPU Status Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
B	C3	TOP			C2	C1	C0	IR	SF	EU	PE	OE	ZE	DE	IE

B: Busy; TOP: 4 2 1 Stack Pointer FPU; C2: FXAM znamienko bitu; C1: ; C0: ; IR: Interupt Request; SF: Stack Fault; EU: Underflow Exception; PE: Precision Exception; OE: Overflow Exception; ZE: Zero Divide Exception; DE: Denormalized Operation Exception; IE: Invalid Operation Exception