

### GPR (General Purpose Registers)

63 QWORD 8B	31 DWORD 4B	15	7	0
<b>RAX</b>	ACCUMULATOR	<b>EAX</b>	<b>AX</b>	<b>AH</b>   <b>AL</b>
<b>RCX</b>	COUNT	<b>ECX</b>	<b>CX</b>	<b>CH</b>   <b>CL</b>
<b>RDX</b>	DATA	<b>EDX</b>	<b>DX</b>	<b>DH</b>   <b>DL</b>
<b>RBX</b>	BASE ADDRESS	<b>EBX</b>	<b>BX</b>	<b>BH</b>   <b>BL</b>
<b>RSP</b>	STACK POINTER	<b>ESP</b>	<b>SP</b>	<b>SPL</b>
<b>RBP</b>	BASE POINTER	<b>EBP</b>	<b>BP</b>	<b>BPL</b>
<b>RSI</b>	SOURCE INDEX	<b>ESI</b>	<b>SI</b>	<b>SIL</b>
<b>RDI</b>	DESTINATION INDEX	<b>EDI</b>	<b>DI</b>	<b>DIL</b>
<b>RIP</b>	INSTRUCTION POINTER	<b>EIP</b>	<b>IP</b>	
<b>RFLAGS</b>		<b>EFLAGS</b>	<b>FLAGS</b>	
<b>R8</b>		R8D	R8W	R8B
<b>R9</b>		R9D	R9W	R9B
<b>R10</b>		R10D	R10W	R10B
<b>R11</b>		R11D	R11W	R11B
<b>R12</b>		R12D	R12W	R12B
<b>R13</b>		R13D	R13W	R13B
<b>R14</b>		R14D	R14W	R14B
<b>R15</b>		R15D	R15W	R15B

### MXCSR REGISTER

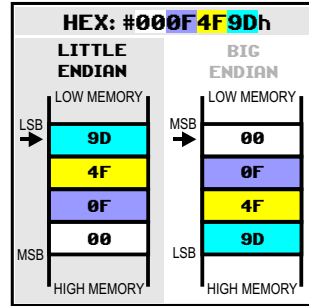
31	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	MM	FZ	RC	PM	UM	OM	ZM	DM	IM	DAZ	PE	UE	OE	ZE	DE	IE		
		Flush to Zero	Rounding Control	Precision Mask	Underflow Mask	Overflow Mask	Divide-by-Zero Mask	Denormal Operation Mask	Invalid Operation Mask	Denormals Are Zeros	Precision Flag	Underflow Flag	Overflow Flag	Divide-by-Zero Flag	Invalid Operation Flag	Denormal Flag		

### EFLAGS REGISTER

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0					
RESERVED FOR INTEL																ID	VIP	VIF	AC	VM	RF	0	NT	IOPL	OF	DF	IF	TF	SF	ZF	0	AF	0	PF	1	CF
																Virtual Interrupt Pending Flag	Virtual Interrupt Pending Flag	Virtual Interrupt Pending Flag	Virtual Interrupt Pending Flag	Virtual Interrupt Pending Flag	Virtual Interrupt Pending Flag	Resume Flag	Nested Task	I/O Privilege Level	Direction Flag	Overflow Flag	Interrupt Enable Flag	Trap Flag (cpu single step mode)	Sign Flag (result is negative)	Zero Flag (result is zero)	Auxiliary Carry Flag	Parity Flag (0=odd 1=even)	Carry Flag			

### Segment Registers

15	0
<b>SS</b>	STACK SEGMENT
<b>DS</b>	DATA SEGMENT
<b>ES</b>	EXTRA DATA SEGMENT
<b>CS</b>	CODE SEGMENT
<b>FS</b>	EXTRA DATA SEGMENT 2
<b>GS</b>	EXTRA DATA SEGMENT 3



15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ST[7]	ST[6]	ST[5]	ST[4]	ST[3]	ST[2]	ST[1]	ST[0]								
0	0	VALID NON-ZERO													
0	1	ZERO													
1	0	SPAC. VALUE (NaN, INFINITY)													
1	1	EMPTY													

### Floating-Point Registers (8 BYTES QWORD 64b)

<b>ST0</b>	79	64	63	<b>MM0</b>	0
<b>ST1</b>	79	64	63	<b>MM1</b>	0
<b>ST2</b>	79	64	63	<b>MM2</b>	0
<b>ST3</b>	79	64	63	<b>MM3</b>	0
<b>ST4</b>	79	64	63	<b>MM4</b>	0
<b>ST5</b>	79	64	63	<b>MM5</b>	0
<b>ST6</b>	79	64	63	<b>MM6</b>	0
<b>ST7</b>	79	64	63	<b>MM7</b>	0

### SSE (16 BYTES)

127	<b>XMM0</b>	0
127	<b>XMM1</b>	0
127	<b>XMM2</b>	0
127	<b>XMM3</b>	0
127	<b>XMM4</b>	0
127	<b>XMM5</b>	0
127	<b>XMM6</b>	0
127	<b>XMM7</b>	0

### SSE2 (16 BYTES) LONG MODE 64-BIT.

127	<b>XMM8</b>	0
127	<b>XMM9</b>	0
127	<b>XMM10</b>	0
127	<b>XMM11</b>	0
127	<b>XMM12</b>	0
127	<b>XMM13</b>	0
127	<b>XMM14</b>	0
127	<b>XMM15</b>	0

### Control registers

63	31	30	29	18	16	15	5	4	3	2	1	0
MSW OLD 286												
CR0 REZIM ADRESOVANIA												
CR2 LIN. ADR. VYPADKU												
CR3 FYZ. ADR. STRANOK												
CR4												
CR8												
CR15												

### Debug registers

31	LIN. ADR. VYKONANIA INT1	0	<b>DR0</b>	
31	LIN. ADR. VYKONANIA INT1	0	<b>DR1</b>	
31	LIN. ADR. VYKONANIA INT1	0	<b>DR2</b>	
31	LIN. ADR. VYKONANIA INT1	0	<b>DR3</b>	
			<b>DR4</b>	
			<b>DR5</b>	
31	STAVOVY REGISTER LADENIA INT1	0	<b>DR6</b>	
31	PRIKAZOVY REGISTER LADENIA INT1	0	<b>DR7</b>	
63	REGISTER ADRESY STROJOVEJ CHYBY	0	<b>MCAR</b>	
63	REGISTER TYPU STROJOVEJ CHYBY	0	<b>MCTR</b>	
63	TESTOVACI REGISTER	0	<b>TR12</b>	
31	OFSET INSTRUKCIE CHYBY	0	<b>FIP</b>	
31	<b>FOP</b> OPCODE	16	<b>FCS</b> SEGMENT	0
31	OFSET OPERANDU INSTRUKCIE CHYBY	0	<b>FOO</b>	
		15	<b>SWR</b>	
31	<b>CWR</b> RIADENIE FPU	15	<b>FOS</b> SEG.ADR.	0
		15	<b>TAG</b> ZNACKY DATO	

<b>FIXED POINT</b>
0000 0
1000 +0.125
2000 +0.25
3000
4000 +0.5
5000
6000 +0.75
7000
7FFF +0.99
8000 -1
9000
A000 -0.75
B000
C000 -0.5
D000
E000 -0.25
F000 -0.125
FFFF -0.01

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Control Word Register CWR FPU Control Register															
			IC	RC	PC	IE	PM	UM	OM	ZM	DM	IM			
			Infinity Control	Rounding Control (zaokrúhľovanie)	Precision Control (presnosť vypočtu)	Interrupt Enable Mask	Precision Mask	Underflow Mask	Overflow Mask	Zero divide Mask	Invalid operand Mask	Denormal operand Mask			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Status Word Register SWR FPU Status Register															
B	C3	TOP	C2	C1	C0	IR	SF	EU	PE	OE	ZE	DE	IE		
Busy		4	2	1		FXAM znamenko bitu	Interrupt Request	Stack Fault	Underflow Exception	Precision Exception	Overflow Exception	Zero Divide Exception	Invalid Operation Exception	Denormalized Operation Exception	

FLOAT 4B | FLOAT 4B | FLOAT 4B | FLOAT 4B |  
 DOUBLE 8B | DOUBLE 8B